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**Important Project of Common European Interest (IPCEI)**

**IPCEI on Microelectronics and**

**Communications Technologies (ME/CT)**

**Safety & Security, Sustainability, and Digital Sovereignty**

**for the European Union of Tomorrow**

**Chapeau Text**

**XX Month 2021**

*“We stress the importance of the digital transformation for European recovery, for its prosperity, security and competitiveness and for the well-being of our societies. […] Furthermore, we underline the need to enhance Europe’s digital sovereignty in a self-determined and open manner by building on its strengths and reducing its weaknesses and through smart and selective action, preserving open markets and global cooperation.” (EU Council, 25 March 2021[[1]](#footnote-2))*

*“Semiconductor components, among them processors, are today embedded in almost everything, from cars and medical equipment to cell phones and networks, and environmental monitoring. They power the smart devices and services we use today. As such, they are the cornerstones of innovation and are central to industrial competitiveness in a digital world. They determine the characteristics of the products into which they are embedded - including security, privacy, energy performance and safety - shaping how Europe’s green and digital transition will unfold.” (Joint Declaration: A European Initiative on Processor and Semiconductor Technologies, 07 December 2020[[2]](#footnote-3))*

*“Europe will only achieve digital leadership by building it on a sustainable digital infrastructure regarding connectivity, microelectronics and the ability to process vast data as they act as enablers for other technological developments and support our industry's competitive edge. Significant investments need to be made in all of these areas that require coordination to achieve European scale”. (2030 Digital Compass, 09 March 2021[[3]](#footnote-4))*

**Executive Summary:**

The proposed IPCEI on Microelectronics and Communications Technologies (ME/CT) addresses important structural challenges to unlock the full potential of microelectronics and communication technologies for the downstream industry and Europe’s society. It is a response to Europe’s need to overcome market as well as coordination failures. Microelectronic components connect our lives by connecting the physical with the digital world. They “Sense, Think, Act, and Communicate". For each of these functions dedicated technologies and specialized know-how as well as high-performance equipment and materials are needed.

The following “Chapeau Text” demonstrates how microelectronics and communications technologies will enable key policy objectives of Europe. The document gives an overview of the current state-of-play of the sector, explains the necessary technologies, and calls for action to create an ambitious, speedy, sufficiently funded, and at the same time realistic IPCEI for Microelectronics and Communications Technology, driven by the needs of industry and European society. In some technological areas, Europe has worldwide competitive positions which must be constantly advanced and expanded, but there are also acute vulnerabilities and dependencies in other areas which must be eliminated or reduced. Therefore, IPCEI brings together industrial stakeholders and RTOs from the whole semiconductor value chain – from raw materials to final systems – and Member States from across the EU. We all together can contribute with our strength, while promoting pan-European collaboration, overcome weaknesses, and create value in all our societies.

Companies and research organizations described below (see XX) intend to participate to an integrated project on Microelectronics and Communications Technologies (the “Integrated Project”) further to the Communication of the European Commission (the “Commission”) on the criteria for the analysis of the compatibility with the internal market of State aid to promote the execution of important projects of common European interest (“IPCEI”) (the “IPCEI Communication”). This Integrated Project meets the eligibility and compatibility criteria described in the IPCEI Communication:

1. It contributes to the objectives of the European Union (“EU“)and has a significant impact on competitiveness and sustainable growth of the EU, addressing societal values,
2. it is an integrated project according to the IPCEI Communication,
3. it has a major innovative content,
4. it generates significant spill-over effects,
5. it is quantitatively and qualitatively important,
6. it involves more than one Member State (“MS”) and co-financing by the direct participants involved in the Integrated Project (the “Direct Participants”),
7. the aid granted is necessary and proportionate.

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# 1. Context and Objectives of the IPCEI Microelectronics and Communications Technologies

## 1.1 Context: Creating Europe’s green, digital, and resilient future

The modern world is inconceivable without microelectronics and communications technologies. Whether it is data processing, the next generation of communication and mobility, applying artificial intelligence and IoT, new technologies for climate neutrality, or the digitization of learning, administration, production and service delivery – none of it would be possible without the pervasive use of the wide variety of microelectronic technologies. In December 2020 EU Member States agreed in a joint declaration[[4]](#footnote-5) to work together to bolster Europe’s electronics and embedded systems value chain to reinforce processor and other semiconductor technologies - which this text summarises as Europe’s Microelectronics Ecosystem[[5]](#footnote-6). Microelectronics is truly at the heartbeat of Europe and indispensable for the Union’s ambition for a greener, digital, more secure, and sovereign society[[6]](#footnote-7). Here, communications technologies provide immediate availability, pervasiveness, and trustworthiness of modern networks for our digital future and wellbeing.

To make this innovation boost possible, we need to orchestrate resources and funding from all over Europe, including private and public stakeholders. In this context, Important Projects of Common European Interest (IPCEI) play a major role in fostering pan-European research and development, design competences, system integration and validation as well as first industrial deployment (FID) of production capabilities and capacity. Europe can only be successful, if the excellent research insights can be transformed into products and services with sustainable value, delivered with competitive edge and at scale. IPCEIs have become a central instrument to maintain the presence of Microelectronics in Europe and to ensure European innovation and competitiveness. An IPCEI on Microelectronics and Communications Technologies (ME/CT) is a large-scale project that will bring together companies and research and technology organisations (RTO) from all over Europe. It combines European knowledge, expertise, financial resources, and the whole ecosystem, including start-ups, SMEs, and large enterprises. An IPCEI on ME/CT addresses the technological performance, sustainability, and societal security challenges of the next decade and results in a clear innovation advantage for Europe. This makes a significant contribution to European technological sovereignty.

In the midst of the pandemic crisis, the EU Commission and EU Member States have put together a massive recovery plan and the Next Generation EU instrument. It goes along with the new MFF 2020-2027, which will be devoted primarily to support the green and digital economy. Also, EU and Member States stressed the need to invest into new digital and green technologies and critical industrial sectors, to overcome structural weaknesses and ensure a futureproof and resilient European economy and society. In order to provide practical support for the Union’s determined agenda, XYZ companies and other entities across the European Microelectronics Ecosystem from XYZ Member States have come together under the banner of “Safety & Security, Sustainability, and Sovereignty for the European Union of Tomorrow”. In their combination, these domains provide a solid foundation for a “green, digital, and resilient Europe”, as Commission President von der Leyen summarized the Union’s overarching challenge for the decades to come.

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| We welcome the vision of the EU Commission to **enlarge the European chip manufacturing footprint to reach a 20% world market share** in cutting-edge and sustainable semiconductors at the end of this decade[[7]](#footnote-8). This IPCEI will help to operationalize this vision and will allow measuring the progress during the lifetime of this IPCEI ME/CT until YEAR X. As such, it will strengthen the European Microelectronics Ecosystem, including European abilities to design at leading edge nodes and will offer a concrete path towards 2nm manufacturing in Europe in the coming decades. |

## 1.2 Objective: Call for Action

European strengths exist in research and development (R&D), semiconductor system and architectural competencies as well as semiconductor materials and manufacturing equipment. However, those can no longer compensate the weaknesses in IP creation, chip design, chip manufacturing as well as assembly, packaging, and test, when compared to microelectronics centres of gravity in the US and Asia. Given China’s, Korea’s, Japan’s, Taiwan’s, and the US’s strong financial and political support for their domestic microelectronics and communication technologies’ value chains, Europe not only has to fill those gaps, but also reinforce existing competitive edge in order to not lose its advantage and be capable of meeting future technological challenges and demands. Neglecting any key part of the entire value chain will lead to structural technological dependency and lack of strategic autonomy.

Of all the instruments available in Europe, IPCEIs have the strongest immediate impact to overcome these weaknesses as they allow to combine significant private and public investments in R&D and FID. To orchestrate and align industry activities with the European objectives, a new “Industry Alliance on ME/CT” will provide the IPCEI governance in close cooperation with the EU Commission and the Member States. This IPCEI on ME/CT is designed to meet the criteria for an IPCEI as communicated by the EU Commission in 2014.

Building on the innovations and progress of the first IPCEI on microelectronics from 2018, this IPCEI on ME/CT will accelerate the Microelectronics ecosystem in Europe. While the first IPCEI has a narrower focus on five core areas, the second IPCEI integrates the whole value chain. This value chain starts with key raw materials and wafers, novel material integration, along with tools and manufacturing equipment, includes to chip design & IP, R&D, manufacturing, packaging, assembly, testing, and ends with system integration and validation, including system software. To avoid overlap with the existing IPCEI, the IPCEI ME/CT is looking at the next generation of technologies to be available in Europe, building on the innovation in the sector which is constantly moving forward. Using the excellent progress of the former one, the IPCEI ME/CT will qualitatively and quantitively extend its scope, give Europe’s industrial resilience in microelectronics the necessary push for the coming decades, and keep European equipment, materials, and communications technologies at the forefront of innovation. At the same time, Europe should not risk its excellent position in the power and sensor technologies, while solely focusing on reducing weaknesses in other areas.

To rightly target the necessary support for innovations and new technologies in the IPCEI ME/CT, it is of great importance to analyse the underlying technological needs and requirements. For some parts of the value chain, such as compute power and memory, “More Moore”[[8]](#footnote-9) is relevant and will now lead to 2nm design and development, and within the coming decade to manufacturing. For several important parts within the semiconductor value chain “More than Moore” and “Beyond Moore” are forming the basis for highly relevant leading-edge innovations. Many growing applications are based on these technological developments, utilizing semiconductor technologies in non-linewidth limited applications in use cases within automotive, communications technology, medical and other fields. Many European semiconductor manufacturers, including both strong and global technology enterprises and smaller specialised companies have created unique capabilities in technologies such as power semiconductors, RF electronics and MEMS. This expertise in diverse fields of semiconductor technology is a source of strength for Europe and should be given the support needed to further develop and exploit these technologies.

These strengths are increasingly strategic, ensuring supply security, economic viability, and data protection sovereignty through mastering of key technology fields. Within these technologies, the key innovations cannot be measures in nanometres, but for example in the innovative use and integration of compound materials (SiC, GaN, GaAs, InP, 2-dimensional materials, advanced photonics, etc,) and additional differentiated features, such as energy and material efficiency, or security design. Cost competitive packaging solutions and the corresponding supply chains are required to bring the innovations to the market. In most of these applications, such as many industrial and automotive applications, logic chips on mature process nodes are still necessary and a strengthening of European chip manufacturing will create new opportunities for the downstream industry.

For the communication sector to fully contribute to an increase in competitiveness of the European value chain, O-RAN networks need to become fully operational, offering increased flexibility, security of supply and security of the data transmitted in an energy efficient manner. Though the European telecommunication private sector has pooled resources and established common goals for O-RAN[[9]](#footnote-10), much remains to be done in research and first deployment of technologies able to offer fully interoperable equipment and tools. Research into network design and solution integration needs to be prioritised. These actions are especially important in the context of 5G/6G network deployment as it would reduce strategic dependency to single-vendor solutions, drive down costs and consolidate European know-how.

Therefore, when approaching the current and future needs of Europe, it is important to cover the whole value chain that constitutes the industry. It includes the following main activities:

* Definition of the requirements driven by the needs of industry
* Technology R&D at universities, RTOs, and companies
* Materials (e.g. advanced compound semiconductor materials), precursors, gases, including eco-design of critical elements and processes
* Tools/equipment (e.g. leading-edge manufacturing equipment)
* Open source and licensable processor IP – isn’t IP relevant for any O-RAN developments?
* Optimize tool landscape for analogue and digital and photonic circuits design, including design tools and design for packaging/test to cope with the increasing complexity challenges
* Advanced chip manufacturing (processors, memories, sensors/actuators, etc.)
* Advanced manufacturing of IC substrates and advanced packaging (IC, IoT, ADAS…)
* Heterointegration of Si and compound semiconductors on chip-, panel- and wafer level
* Monolithic integration of novel semiconductor materials
* Testing, assembly, packaging, and other post-fab operations
* Hardware-Software integration
* Advanced validation tools and measurement systems for microelectronics and electronic-based systems
* Education and training

The achievements of this IPCEI will be measured in an increased European manufacturing footprint within the global microelectronics and communications technologies industry, and in an increase of European IP ownership by strong design competencies to further enable for Europe’s digital decade. To achieve this, we need significant investments in the entire value chain ensure best performance, lifetime, safety and security of electronic-based systems e.g. in mobility or telecommunications or environmental monitoring applications. Based on the needs of industry from automotive to telecom to MedTech/Life Sciences, this requires continued alignment across industry sectors, including co-working models with centres of competence and research.

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| **If the combination of processor and memory is the brain of a computer (“think”), then other important types of semiconductors stand for the organs of perception - eyes, noses, skin, tongue, and ears (“sense”)** connected via nerves to form a networked system**.** Modern systems, be they cars, smartphones, smart meters, industrial IoT devices, satellites, or Industry 4.0 systems, need both dimensions to function. Without the data from these semiconductor devices, the processor would have nothing to process. Work and performance can only be achieved when the **body and muscles (“act”)**, networked with the brain via **strong nerve pathways (“communicate”)**, work together effectively at lowest energy consumption and environmental impact possible. |

We welcome the ambitious vision of the EU COM on leading-edge microelectronics. This IPCEI can contribute on leading-edge nodes (2nm) with projects in the areas of design, IP-generation, process development, as well as in semiconductor manufacturing equipment and materials leveraging existing European strength (EUV lithography, 3D integration, advanced packaging, photo masks, semiconductor materials, and test structures). Expanding production capacity in Europe is currently best achieved by strengthening existing competences, because it must be centred around market and customer demands to create real value for Europe and create spill-over effects for society. The best way forward includes (1) expanding technology nodes capacities in the 45-22nm range and down to 12nm, which play an important role and have strong demand by European downstream industries and beyond, (2) pushing competences in chip design, equipment, and materials for leading-edge semiconductor technology towards 2nm and below, and (3) inviting leading-edge semiconductor manufacturers to build fab(s) in Europe. At the same time, investments into (4) Open RAN network design and aggregation and (5) Open RAN equipment manufacturing need to be backed to unlock the full potential of sustainable, futureproof communication networks.

Currently industry is experiencing significant supply shortages and dependencies on foreign production, which indicates market failure and leads to production disruptions in many industrial sectors across Europe. Considering the proposed range of investments for this IPCEI on ME/CT, it will be most effective and efficient to support capacity extensions at foundries and companies manufacturing in Europe for Europe, including advanced compound power semiconductor and advanced RF-semiconductors technologies, integrated photonics, advanced packaging, IC substrate technology, testing as well as sustainable sourced materials and precursors, and to develop design competences for leading node technologies.

With increasingly more complex systems, the semiconductor supply chain is facing new challenges requiring removing bottlenecks, shorten lead-times and enhance flexibility of production capacity. This requires a common approach in implementing a “digital industrial data space” to help the entire semiconductor supply chain to implement or improve the appropriate industry standards and accelerate digital collaboration. Implementing such a digital transformation roadmap throughout the semiconductor value chain, will in turn significantly raise the attractiveness of the European high-tech ecosystem to compete on a global scale, including small and medium sized manufacturing companies.

To address the above challenges Europe needs a roadmap for the next 10-15 years, which should be regularly measured against actual requirements and can be adjusted if necessary. A bundle of measures must be launched, addressing European demand and European supply, while the right timing, sufficient investment, and the available workforce must be considered.

## 1.3 Strategic Importance and Contribution to EU Objectives:

### 1.3.1 Strengthen Europe’s Microelectronics and Communication Ecosystems

Only by significantly extending its overall footprint in the global microelectronics domain the EU will be able to achieve its ambitious targets. Europe’s dependence on external suppliers and technologies for microelectronics and their manufacturing has steadily grown over the past 30 years to a point that Europe has become vulnerable in some specific areas of the semiconductor domain. Therefore, to remain globally competitive, Europe must find a decisive answer by creating the conditions for a strong, future-ready, profitable, and crisis-proof European value chain for microelectronics able to supply electronic components and systems for important downstream industries in Europe.

Within the field of communication technology, the most promising and critical components are necessary in the field of mobile/radio network technology and optical transmission technology, as these technologies are vital and mission critical for a modern and sustainable digital economy. Modern economies do require and rely on modern mobile networks and the latest technologies applied herein.

The era of 5G and 6G networks is characterized by an ongoing trend towards cloudification and disaggregation of networks, meaning that many previously hardware based communications systems are now being implemented as SW and by breaking up the integrated HW/SW components into more modular and commoditized pieces of infrastructure. This trend is very much reflected in the Open RAN architecture, which well embraces both trends and has to be regarded as basis for future mobile networks.

It is therefore inevitable for Europe’s industry to engage on Open RAN and to address the full set of HW and SW components necessary to get to an end-to-end supply chain, made in Europe.

The IPCEI therefore welcomes initiatives which contribute to the design and deployment of Open-RAN technology across the full span of necessary technology. In this range of technology microelectronics plays one of the most important roles, as many of the complicated network functions are deeply integrated into chipsets. Still a network requires more than chips only and in order to reflect the importance of networks for the well-being of the societies the scope of the IPCEI covers explicitly also the network integration layers above the chip level.

Having European horses in the technology race as bargaining chips ensures beneficial mutual dependencies in the global semiconductor and communications supply chain. This will leverage investments in the whole value chain, and it should foster ~~semiconductor~~ start-up companies. This will stimulate novel technologies reaching the market, help to counter market-failure and reduce the risk of disruptions by external shocks. However, political decisions should not be directed at curtailing the global value networks of the semiconductor or communications industry. Even well-intentioned measures in this context can lead to significant welfare losses. In a functioning global production network, not everyone can and must be able to do everything alone, but Europe must become more aware of its strategic control points, which it can leverage in a geopolitical reality.

The challenges confronting the EU economy are plainly in sight when it comes to crisis-proof supply of microelectronics from around the world. In 2020/21, access to chips and systems has turned into a chokepoint for every industry in any European sector. Although Microelectronics will rely on world-wide trade and cooperation, previously taken-for-granted global supply chains are fraying: The impacts of climate change – e.g. through the effects of extreme weather events on critical infrastructures as energy supply or water management – geopolitical tensions, resource scarcity, and unforeseen global trade disruptions are putting the chip supply chains under pressure. At the same time, other world regions pursue ambitious industrial policies, strengthen their domestic actors, and onshore foreign producers. Therefore, Europe should develop resilient and crisis-proof supply chains for European and world markets. While Europe is still in a strong position in the communications technologies space, this position is endangered by increased market entry of foreign producers and new technological innovations. Therefore, it is also time to strengthen Europe’s communications technologies supply chain.

The European Union aims for the twin green and digital transition. Therefore, EU policies for the Green Deal and Digital Decade want to create a framework which triggers new solutions to make Europe more resilient and fit for the coming decades. New digital technologies provide the solutions for increasingly complex mobility needs, intelligent manufacturing, smart cities and communities, the operation of critical infrastructures in the areas of energy supply, data-/telecommunication, and health, the increasing level of digital networking and global climate protection. Microelectronics, integrated photonics, and communication technologies are the key enabler for Europe’s future economic prosperity and the provider of the innovative digital solutions needed to address Europe’s societal challenges[[10]](#footnote-11). Without a strong and competitive European Microelectronics and Communications Ecosystem the ambitious targets of the twin green and digital transition cannot be achieved! With the Green Deal as a guideline Europe can lead the path for a greener microelectronic ecosystem.

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| European leaders recognized the need for a broader Microelectronics Ecosystem[[11]](#footnote-12):  ***“The signatory Member States agree to work together in order to bolster Europe’s electronics and embedded systems value chain****. This will include a particular effort to reinforce the processor and semiconductor ecosystem and to expand industrial presence across the supply chain, in order to address key technological, security and societal challenges. We agree to consolidate and build on Europe’s position in areas of proven expertise and aim to establish advanced European chip design capabilities and production facilities progressing towards leading-edge nodes for data processing and connectivity.”* |

To extend competitiveness, the European actors in various application domains need to secure access to leading-edge technology nodes. Enabled by European competences in semiconductor manufacturing equipment and materials, Europe can push the industry to accelerate towards more advanced technology nodes, and at the same time strengthen its position within a global supply chain that is confronted with increasing geo-political tensions and frictions.

The European semiconductor manufacturing equipment and materials industry, and its world-class high-tech supply chain, is well positioned to (continue to) play a key role in this and capitalize on the expected growth in the sector. The packaging industry, which is currently mainly outside of Europe must be strengthened in Europe, to make a restart with advanced packaging and outstanding substrate technologies. Manufacturing equipment and materials is an essential European strength in the global microelectronics industry, thanks to its world-leading actors in lithography, optics, metrology, bonding and assembly, wafer-level packaging, atomic layer deposition and epitaxy areas. Therefore, equipment is an important leverage point to negotiate better conditions overall for EU players in the microelectronics supply chain. The strong synergy between the development lines of RTOs and equipment manufacturers is demonstrated by the number of tools that are sold worldwide, developed and tested in their cleanrooms.

Process technology pilot lines are extremely important tools for providing accelerated feedback on the product roadmaps of the European manufacturing equipment sector. Additionally, they enable semiconductor manufacturers to develop essential manufacturing process technologies and support efficient transfer of high-value process technology modules to a high-volume manufacturing environment. This is valid for advanced-node equipment as well as Back-End manufacturing equipment, as typical edge-of-the-cloud applications require application-specific advanced packaging and heterogeneous integration combined with state-of-the-art advanced node technologies.

### 1.3.2 Microelectronics and Communications Technologies are the technological foundations for a modern Europe

This proposed IPCEI is driven by the needs of European industry to assure its pace of innovation and competitiveness. Both require unconstrained access to trustworthy microelectronics components and related hardware and software systems, as well as communication systems.

The IPCEI will contribute to several EU goals, amongst which the EU Industrial Strategy’s intention to reduce strategic dependencies in key areas, including semiconductors. It will also support the goals expressed in the Digital Decade communication, specifically in regards to secure and performant digital infrastructure covering connectivity, microelectronics and the ability to process vast data. An innovative, strong communication sector based on O-RAN technologies will support the ambitions set out in the 5G Action Plan (*ensure uninterrupted 5G coverage in urban areas and along main transport paths by 2025*) considering that the industry expects to be able to support a significant share of 5G deployment once O-RAN technologies reach the performance levels of classic RAN.

The IPCEI on ME/CT is the opportunity to reinforce a future-proof European industry footprint by securing critical design, sustainable supply, and advanced manufacturing capabilities along the entire value chain. From the essential system definition down to the fundamental tools for manufacturing, Europe has the capability and the ambition to be a strong player.

Applications such as electric and autonomous driving, wearable medical diagnosis, innovative manufacturing systems in industry (Industry 4.0), smart/advanced infrastructure, and next-generation communication technologies (5G advanced and non-terrestrial, optical interconnects, and 6G) will require microcontrollers and microprocessors with particularly high computing power, high data exchange capacity and at low power consumption as foundation for modern networks – especially when functionalities such as machine learning and artificial intelligence are integrated. Fundamental improvements in e-mobility towards improved efficiency and less resource use require new motor technologies which in turn demand better sensors. Growth of the robotic market into the domains of healthcare and personal service robots demands substantial improvement of robot capabilities at significant reduction of cost. Only new sensor and integration technologies can support the development of new robotic systems which are required to support the ageing society.

The transition to industry 4.0 for the industrial sector is a major challenge involving numerous SMEs in Europe. This transition will benefit from new European capacities in microelectronics front-end, but also back-end including “System in Package” capabilities. In addition, by 2025 there will be more than 50 billion networked devices on the market worldwide with a data volume of 79 Zettabytes to be processed. These devices need to be interconnected by a high-performance communication network. This is where edge processing and O-RAN networks will play a decisive role. It must be ensured that the applications are functionally safe and cyber secure, but at the same time can be operated in an energy-efficient manner. Here, technology nodes for processors in the ≤10nm range come into play. Chip solutions in these structure sizes make it possible to create up a European end user market for computing platforms for electromobility, digital factories and 6G infrastructure. Additionally, as the overall part of Industry 4.0 and 6G-application will have a significant impact on the energy consumption of the industry and society, energy/material efficiency in driving this electronic infrastructure will take a more and more important role.

Applications in automotive, especially for autonomous driving, - complemented with ML and AI functionalities - will require high-end microcontrollers and microprocessors with very high computing power, while being safe, cybersecure and energy efficient at the same time. The next generation vehicle architecture, where these chips play a key role as brains of the car, will also need chip solutions in the 5/2nm range to deliver on these requirements and enable EU industry to develop/provide the necessary computing platforms to be at the forefront in innovations. In addition, these high performant chips will be used as edge devices in the car to manage the tremendous amount of data provided by the highly increased number of sensors, the latter ones being a strength of the European industry. Additionally, the “electrification” of the car results in a substantial increase of the electronic content in today’s and future cars with energy efficient power electronic circuits for driving the electric vehicles of future mobility platforms. These power electronics will need leading edge compound semiconductors for future electric vehicles of the next level.

At the same time, in the industrial automation, machinery, and plant engineering sectors the quantities for volume production and NRE costs in leading edge semiconductor technologies require more mature technology nodes, which yield high amounts of dies-per-wafer. For example, for smart power technologies analogue/mixed signal capabilities are of key importance and do not require “More Moore” but novel materials, innovative designs, and improved synergies on system level.

The communication sector is an excellent example how Europe can retain its leadership from the 4th and 5th generation radio communications technology in the upcoming 6th generation (6G) communication technology and infrastructure, as well as in complementary wireless low-power short range technologies enabling efficient IoT implementations. To make 5G and 6G technology not only available for consumers (smart phones), but also for industrial applications, the technology must be smoothly integrated in existing and upcoming industrial communication systems. Access to that technology for both large and small enterprises must be simple and cost effective. 5G and 6G must be made Industry 4.0 compliant and combining both terrestrial and non-terrestrial networks. As a matter of fact, the European communication industry has played a leading role in the standardization and development of the 2G/3G/4G/5G communication technology, including the corresponding IP. USA and Asian countries are investing Public funds to support their industries to be able to compete in 6G enabled networks business. Europe needs to match this by supporting local vendors in 6G, RDI speed-up to generate IP, define global standards, develop key technologies and related micro-electronics, ensure highly adaptable end-to-end communications solutions, and reliably guarantee cyber security through innovative approaches. This is important to protect the mobile networks and billions of connected devices against hacking, data theft and sabotage. This will require advanced communication infrastructure, devices and applications provided by the European microelectronics and communication technologies industry. Also, virtualisation of hardware and interoperable interfaces for communication systems like cloud-native RAN and core networks will require high-performance processors, software integration and application ecosystems. For the first time with advanced 5G and 6G, commercial communication standards will use millimetre wave frequency bands in Europe. Manufacturing processes and components throughout all production layers are currently not available for these frequencies and need to be developed for commercial mass production, including R&D and test & measurement solutions.

Photonics technologies provide highly integrated optical communications products based on optical System-on-Chip technology, enhancing very energy efficient data transmission over longer distances and providing provide more bandwidth to end-users. Data centres today are scaling up to meet the continuous growing demand for higher bandwidths. Integrated photonic optical transceivers overcome this challenge by creating more energy-efficient photonics-based products that provide high transfer speeds against a lower energy footprint. To position Europe well for these communication challenges, it is imperative to establish technologies, design, and develop infrastructure-, system- and test solutions in a leading and self-determined manner. Although the 6G roll-out will only happen from 2028 onwards, the IP generation and technology development starts now. Let’s make 6G “made in Europe”!

While Europe still shows strength in some areas of the communication sector the emergence of open interfaces forces a new level of efforts in the creation of secure network functions. In the safety and security area, Europe must extend its technological leadership. Functional safety in automotive, communication and industrial areas is one of the key strengths of European IC designers and manufacturers and will be key for autonomous and safe driving. Security processors designed in Europe have set worldwide standards and can be considered as global benchmark. Based on these European strengths, we have all the means to master the upcoming challenges of cyber security: quantum computers can perform complex computations that will render most, if not all, of today's public-key cryptography solutions vulnerable and thus unusable with little effort. To date, the necessary components, and implementations to protect any systems from quantum compute-based hacking are not available on the market and need to be developed. “Beyond Moore”, the synergy of “More Moore” and “More than Moore” will be the solution. In this domain there will emerge positive spill-over effects from the IPCEI on ME/CT on other European Projects, as the EuroQCI[[12]](#footnote-13).

All semiconductor applications mentioned above need pure materials as prerequisites. For future chip generations and new application segments, quality, purity, sustainability, and manufacturing costs must be further improved to make Europe a centre of innovation and stable technological development.

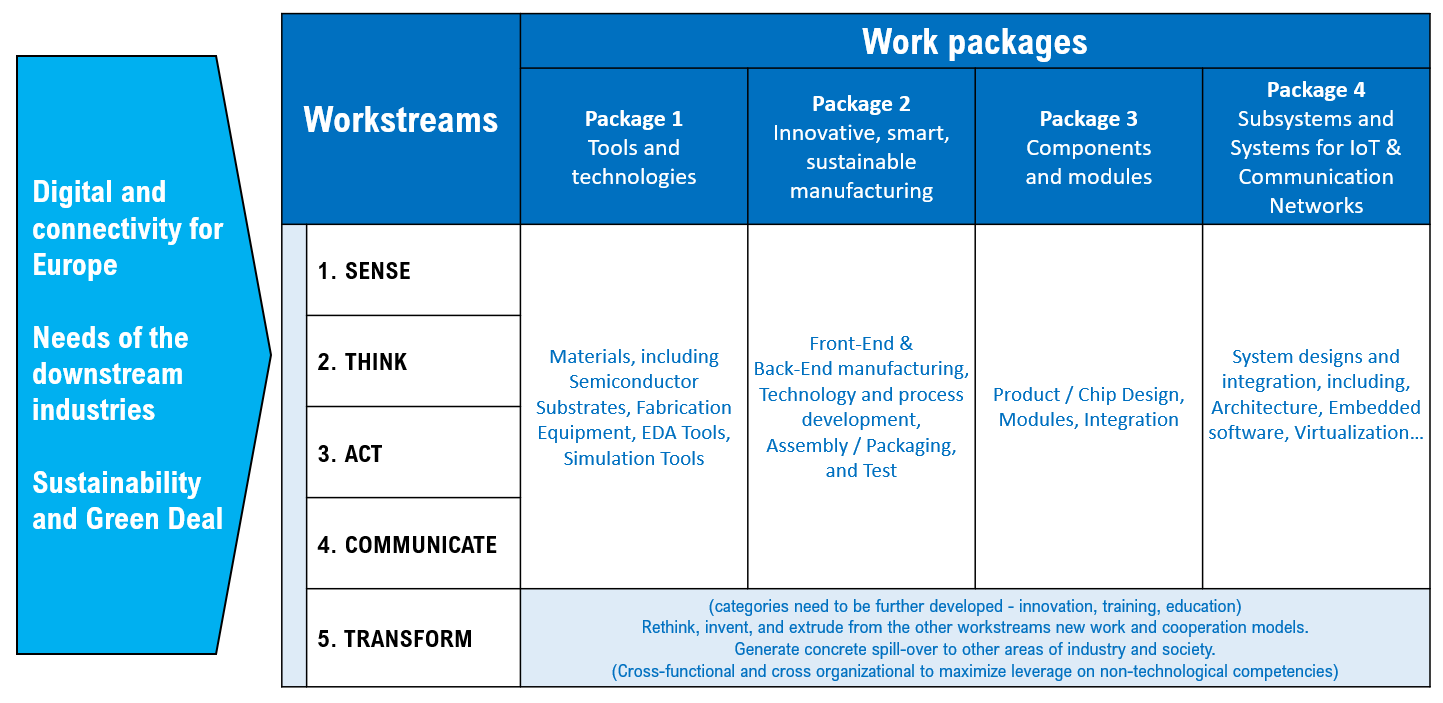
|  |
| --- |
| **“More Moore (MM)”** refers to the exponential doubling of the number of transistors per mm2 approx.- every two years as a measure of the chip’s performance. It is generally expressed as continuous scaling which took the industry from the 180nm node in 1999 (followed by 130nm, 90nm, 65nm, 45nm, 32/28nm, 22/20nm, 16/14nm, 12nm, 10nm and 7nm) to the 5nm node in 2020. Industry Roadmaps are showing this trend to continue well into the next decade approaching the 1nm node. Likewise, performance per area, power and cost of chips goes up, and investment cost is measured in Billions.  **“More than Moore (MtM)”** refers to the concept which foregoes continuous and costly scaling and looks for technology advances by focusing on specific chip features like analogy, RF, MEMS and sensors, opto, power devices, mixed signal devices, accelerators, packaging etc.  **“Beyond Moore (BM)”** is a concept that overcomes the traditional and increasingly unsuitable split between MM and MtM but proposes to merge elements from both realms as required, possible and affordable to provide fitting solutions. BM has a functional innovation of more than 10x from generation to generation. |

Europe must master fundamental innovation challenges that are the result of the megatrends of the first half of the 21st century which are driving advances today and in the near future: communication technologies (5G/6G including wireless and optics), smart and green mobility (electrification), power efficient data management and high degree of automation including “safe” artificial intelligence and autonomous driving.

A competitive European microelectronics and communications technologies industry aiming to provide solutions for these verticals must consider the following major elements:

* Functional innovation for the end user’s benefit,
* technology push to implement such functional innovation into a product,
* supply chain control via manufacturing of key microelectronic products and the associated systems, but also materials and production equipment, as well as advanced packaging,
* thorough validation/testing of (micro)electronics-based components and systems with respect to performance, lifetime, safety, and security
* AI based advances in design methodologies from System to Product, to speed up Time to Market by consequent use of Digital Twin Prototyping
* efficient use of resources for a sustainable and circular economy,
* creating competitive ecosystems for attracting highly educated international talents
* proven end-to-end optical and radio communications solutions
* training, education, and development of the staff/experts necessary for these activities.

All these elements are interlinked with each other and require careful balancing to achieve maximum traction in an international competitive situation. The systems that are designed for the end users’ benefit typically consist of four major building blocks “Sense, Think, Act, Communicate” as functional elements that relate to sensors, high performance processors, microprocessors including artificial intelligence, actuators and communication means for secure data exchange. Together they connect our lives and physical world with the digital world of data. Co-design and fine-tuned interaction of these functional elements is essential to generate the intended performance and function at lowest cost and lowest environmental impact possible.

**Table 1: Workstreams and overall project structure**

Therefore, the IPCEI ME/CT will apply these building blocks “Sense, Think, Act, and Communicate, as workstreams, together with the fifth workstream “transform”, which focusses on new models of work and cooperation, keeping education up to date to ensure the availability of perfect skilled employees as well as spill-over effects of the other workstreams (see Table 1 & Chapter 2). The workstreams are crossing four vertical work packages, representing part of the value chain, to include the whole European Microelectronics and Communications Ecosystem. The necessary technologies are defined by needs of the European downstream industries and the common European interest, defined by the goals of the EU Commission for digital and connectivity, as well as Green Deal and sustainability.

### 1.3.3 Integrating the whole Microelectronics and Communications Ecosystem

A properly aligned and cooperative set-up between the associated levels of the microelectronic value chain and the different players in their respective fields under the umbrella of an IPCEI on ME/CT will result in innovative, energy-efficient, highly performant and trustworthy solutions that will meet the needs of the European industry and society as it transitions towards a green, digital and globally competitive future. Here also training, education, and development of employees and experts is essential for the future of this high-tech sector. Strengthening STEM education and closing the gender gap in technology subjects are just two urgent matters that need to be addressed. Microelectronics and communications technologies are an important enabler functions and are therefore highly attractive for young experts. This IPCEI will create spill-over effects to the EU Pact for skills, as microelectronics has been chosen as one of the three industrial sectors to be considered[[13]](#footnote-14).

The IPCEI ME/CT assembles actors from all elements of the value chain, including SMEs. Special emphasis will need to be put on the high investment requirements for complex product development along the entire value chain and industrialization at scale. It will take an ambitious, sustained and, above all, joint effort of industry, Member States and the European Commission to empower the European microelectronics and communication sector in such a way that it can fulfil its role as a key enabler for downstream industries.

## 1.4 Realization Plan

Countries have come together to achieve these goals to compensate for the market failure for European user industries.

The integrated project meets the eligibility and compatibility criteria described in the IPCEI Communication:

* It contributes to European Union objectives and has a significant impact on competitiveness and sustainable growth of the EU, addressing societal values (1).
* It is an integrated project according to the IPCEI Communication (2).
* It has a major innovative content (3).
* It generates significant spill-over effects (4).
* It is quantitatively and qualitatively important (5).
* It involves more than one-member state and co-financing by the direct participants (6).
* The aid granted is necessary and proportionate (7).

# 2 Description of the integrated project

This chapter gives a detailed description of the integrated project. Direct Participants have been selected by MS through open and transparent procedures (2.2). They will address the main technical challenges (2.3) of the downstream industries. The Integrated Project addresses five complementary workstreams (2.4 - 2.8). The individual projects gathered in the WS are necessary and complementary and the WS themselves are necessary and complementary (2.9). The complementarity of the WS is further demonstrated by the governance rules of the Integrated Project (2.10).

## 2.1 Differences and Synergies between the 2018 IPCEI on Microelectronics and the IPCEI ME/CT

The 2018 IPCEI on Microelectronics had a narrow focus on five core areas: energy efficient chips, power semiconductors, smart sensors, optical equipment, and compound materials. The IPCEI ME/CT has a broader focus that includes the entire value chain from materials to system integration.

The previous IPCEI did not include the newest generation of power semiconductors. However, this generation has significant benefits compared to the previous generations due to the significant development in the materials used in the power semiconductor industry since the last IPCEI.

This includes the newest generation of semiconductors based on silicon carbide (“SiC”) technology. The use of this technology enables greater efficiency of the semiconductors. As key element of power electronics SiC semiconductors are crucial to all machinery powered by an electric engine and due to the higher efficiency especially for particularly complex applications. Therefore, SiC semiconductors can contribute significantly to the European objective of a green and digital transition as, for example, they allow for a greater range and higher performance of EVs while size of batteries and charging time will decrease. Another example are the renewable energies, where SiC semiconductor can significantly improve the efficiency of wind and solar power converters.

## 2.2 Detailed description of the Direct Participants

Direct Participants have been selected by MS further to open and transparent procedures (2.1.1). They have all submitted an individual project in the field of ME/CT and have been selected by their MS as beneficiaries of State aid in the context of this Integrated Project following a competitive, transparent, and non-discriminatory procedure. In addition, in accordance with pt. 20.a) of the IPCEI Communication, the Integrated Project has been designed to make it possible for all interested MS to participate. This is illustrated by the fact that different types of individual projects with very different amount of public support have been selected by the participating MS. This is further illustrated by the conditions set for the possible entry of additional Direct Participants within the Integrated Project after the clearance by the Commission.

A detailed list of all the participants and their company descriptions can also be found in the ANNEX (X) on pages (X).

The RDI and FID works carried out by the Direct Participants will be organized along the workstreams (“WS”) identified below within and across which they will collaborate. These WS address the different topics among the value chain within which challenges must be overcome for the Integrated Project to be successful.

Each WS is centred on key stages of the Microelectronics Ecosystem. The Direct Participants have considered the following benefits which have been key factors in joining. Without these positive considerations, no such Integrated Project would have materialized, and the collaborations described below would have been fewer and shallower (if any):

* Aggregation/cross-fertilization effect: the elevated number of partners with differing backgrounds in the industry and R&D brings together a wide pool of expertise along the value chain. This scope and diversity of knowledge and know-how which will be directly and indirectly pooled together will accelerate the speed and deepen the quality of the progress achieved within the many collaborations of the Integrated Project.
* Pulled by the best: due to the well-recognized world-class status of several participants to this Integrated Project which have an established track-record of differentiation with high-quality and high-technology products and services, expectation on the collaboration deliverables will be set at a high level, hence ensuring the quality of the deliverables.
* Developing the EU ecosystem: this Integrated Project is giving the opportunity to create links with EU players of different size and geographic footprint which would otherwise not have been created, as companies acting individually would have preferred establishing relationships with several existing non-EU players.
* Better focus: this Integrated Project will give several actors the opportunity to jointly identify necessary areas of progress in the advanced materials and recycling industries, and therefore give a coordinated message to the related RDI teams on where efforts should focus.
* Widening the pool of potential partners: through this Integrated Project, which is to a large extent an outcome of the European ecosystems on ME/CT, several participants discovered the existence and activities of some partners with potential they were unaware of and created the relevant collaborations.
* The assistance of a framework: the necessary duration of some of the collaborations is such that a framework is needed to help Direct Participants make the required long-term commitments.
* Reduction of the financial risk: the positive financial return of many projects is too remote and/or too risky to secure a “go-ahead” decision; public support is therefore required to allow the Direct Participants to start their individual projects.
* Elimination of showstoppers: some actors would not have been created without the public support which the participating MS have committed to provide; their related individual projects would therefore not have existed without the Integrated Project.

The necessity and complementarity of the individual projects and the collaborations entered by the Direct Participants are described within each WS with more details.

2.2.1 Open selection of the direct participant

MS 1

[Explanation on selection process]

**FRANCE**

The French authorities have launched two parallel calls for expressions of interest to select companies to participate in projects along the entire value chain of major innovations in the field of nanoelectronics and its applications and in the field of connectivity.

* The call for projects on nanoelectronics was opened on XX/XX/XXXX and closed on XX/XX/XXXX. XX applicants submitted an application and XX were pre-selected following hearings on XX/XX/XXXX.
* The call for projects on connectivity was opened on XX/XX/XXXX and closed on XX/XX/XXXX. XX applicants submitted an application and XX were pre-selected following hearings on XX/XX/XXXX.

## 2.3 Main Technical Challenges and their Application Domains

Technical requirements of the user industries with the associated challenges

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## Workstreams Sense

### Objectives and Challenges

#### 2.4.1.1 Objectives of the WS Sense

[presenting the objective]

#### 2.4.1.2 Challenges of the WS Sense

Challenges regarding RDI in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

Challenges regarding FID in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

### 2.4.2 Overall Presentation of the Direct Participants of WS Sense

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| --- | --- | --- | --- |
| Company name | Financing MS | Size of company | Project description |
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### 2.4.3 Collaborations of the Direct Participants with other indirectly involved partners

| Name of indirectly involved partner | Country | Connected to direct participant | Main activities contributed to IPCEI | SME or LE or RTO |
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## Workstreams Think

### 2.5.1 Objectives and Challenges

#### 2.5.1.1 Objectives of the WS Think

[presenting the objective]

#### 2.5.1.2 Challenges of the WS Think

Challenges regarding RDI in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

Challenges regarding FID in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

### 2.5.2 Overall Presentation of the Direct Participants of WS Think

|  |  |  |  |
| --- | --- | --- | --- |
| Company name | Financing MS | Size of company | Project description |
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### 2.5.3 Collaborations of the Direct Participants with other indirectly involved partners

| Name of indirectly involved partner | Country | Connected to direct participant | Main activities contributed to IPCEI | SME or LE or RTO |
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## 2.6 Workstreams Act

Power technologies, electronic components and systems are key decarbonization factors to tackle with the global warming. Improving the Energy efficiency will be a critical challenge for a wide range of future electronic power application , where avoiding loss is top priority, e.g. for HPC data centres, electric vehicles, digital health systems, automated manufacturing, industrial solutions, efficient power conversion for smart grid and renewables.

The main challenge for multiple industry sectors is the generational transformation towards electrification aimed at ultimately achieving climate neutrality. In particular, the electrification of the automotive is a key pillar to reduce greenhouse gas emissions as a 90% reduction in transport emissions is needed by 2050 to achieve climate neutrality.

In this context, the main objective of work package 2 of this workstream is the improvement of the efficiency, quality, purity, sustainability, and manufacturing costs of power semiconductors to the requirements of sectors that are transitioning towards electrification, in particular, the automotive industry.

A further objective of this work package is to contribute to an increase in supply chain assurance for compound semiconductors in Europe. In the context of the current semiconductor shortage that i.a. impacted the automotive industry where productions had to be kept idle, a multi-source, mature supply chain can form an important building-block for supply chain assurance of compound semiconductors and the goal of Europe’s resilience.

Moreover, it is an objective of this work package to elevate European technology leadership in the transformation from combustion technology to electrification by establishing one for the most advanced production facilities for SiC wafers in Europe.

With regard to the newest generation of SiC semiconductors the major challenge lies in optimizing the efficiency and integration of SiC semiconductors

### 2.6.1 Objectives and Challenges

#### 2.6.1.1 Objectives of the WS Act

The objective will be to develop and implement beyond the state-of-the-art's innovative technologies for smart power and discrete silicon devices, to increase energy efficiency everywhere. This will allow designers to create circuits with higher density, better efficiency and greater reliability while achieving smaller form factors for lower cost installation at system level.

The additional benefits of wide-bandgap semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) will further push the monolithic integrations solutions enabling a much smaller bill of material and a faster design cycle,

#### 2.6.1.2 Challenges of the WS Act

* The challenges to better serve the electrification and digitalization trends with progress beyond state of the art for semiconductor content will be:
* New semiconductors materials and substrates for power technologies
* Innovative technology options and designs for Power Silicon components
* Innovative technologies and designs for WBG-based power components
* Dedicated driver and logic to control WBG-based power devices
* Dedicated packaging technologies and processes for power components
* New solutions to lead in embedded processing
* Development of analogue, sensors and actuators for power & energy management
* Develop industrial capacity dedicated to automotive power modules and systems

Challenges regarding RDI in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

Challenges regarding FID in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

### 2.6.2 Overall Presentation of the Direct Participants of WS Act

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| Company name | Financing MS | Size of company | Project description |
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### 2.6.3 Collaborations of the Direct Participants with other indirectly involved partners

| Name of indirectly involved partner | Country | Connected to direct participant | Main activities contributed to IPCEI | SME or LE or RTO |
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2.7 Workstreams Communicate

### 2.7.1 Objectives and Challenges

#### 2.7.1.1 Objectives of the WS Communicate

[presenting the objective]

#### 2.7.1.2 Challenges of the WS Communicate

Challenges regarding RDI in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

Challenges regarding FID in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

### 2.7.2 Overall Presentation of the Direct Participants of WS Communicate

|  |  |  |  |
| --- | --- | --- | --- |
| Company name | Financing MS | Size of company | Project description |
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### 2.7.3 Collaborations of the Direct Participants with other indirectly involved partners

| Name of indirectly involved partner | Country | Connected to direct participant | Main activities contributed to IPCEI | SME or LE or RTO |
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## 2.8 Workstreams Transform

### 2.8.1 Objectives and Challenges

#### 2.8.1.1 Objectives of the WS Transform

[presenting the objective]

#### 2.8.1.2 Challenges of the WS Transform

Challenges regarding RDI in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

Challenges regarding FID in this WS will be:

* Challenge 1
* Challenge 2
* Etc.

### 2.8.2 Overall Presentation of the Direct Participants of WS Transform

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| --- | --- | --- | --- |
| Company name | Financing MS | Size of company | Project description |
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### 2.8.3 Collaborations of the Direct Participants with other indirectly involved partners

| Name of indirectly involved partner | Country | Connected to direct participant | Main activities contributed to IPCEI | SME or LE or RTO |
| --- | --- | --- | --- | --- |
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## 2.9 Necessity and Complementarity of the Projects

Compliance of the Integrated Project with EU competition law rules: The Direct Participants are active in different fields of the ME/CT ecosystem and will collaborate with each other to develop an innovative ME/CT project within the EU. Such collaborations are essential to achieve the goals of the Integrated Project and comply with the requirements of Article 101 of the Treaty on the functioning of the EU (“TFEU”). In addition, where necessary, the Direct Participants concerned have completed or are in the process of completing the merger control requirements

### 2.9.1 Summary of the participation of the Direct Participants to the WS

The Direct Participants will collaborate within and/or between the above-mentioned WS. Each Direct Participant’s individual project constitutes a single project which is part of the Integrated Project. Table XX below summarizes the participation of the Direct Participants to the four different WS.

**Table XX:** Summary of the WS of the IPCEI on XXXX and the involvement of each Direct Participant

| **WS SENSE** | **WS THINK** | **WS ACT** | **WS COMMUNICATE** | **WS TRANSFORM** |
| --- | --- | --- | --- | --- |
| **Name of the company & Financing MS** | **Etc…** | **-** |  |  |
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**Table XX** below summarizes the intra-WS and inter-WS collaborations that will take place in the framework of the Integrated Project.

**Table XX:** Summary of the different collaborations taking place in the framework of the Integrated Project

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **WS** | **Number of collaborations** | **Collaborations intra WS** | **Collaborations inter WS** | |
| **WS** | **Number of collaborations** |
| **WS SENSE** |  |  | WS THINK |  |
| WS ACT |  |
| WS COMMUNICATE |  |
| WS TRANSFORM |  |
| **WS THINK** |  |  | WS SENSE |  |
| WS ACT |  |
| WS COMMUNICATE |  |
| WS TRANSFORM |  |
| **WS ACT** |  |  | WS SENSE |  |
| WS THINK |  |
| WS COMMUNICATE |  |
| WS TRANSFORM |  |
| **WS COMMUNICATE** |  |  | WS SENSE |  |
| WS THINK |  |
| WS ACT |  |
| WS TRANSFORM |  |
| **WS TRANSFORM** |  |  | WS SENSE |  |
| WS THINK |  |
| WS ACT |  |
| WS COMMUNICATE |  |
| **Total** |  |  |  |  |

There will be numerous collaborations within this Integrated Project which would not occur to this extent without such project. These agreed non-exclusive collaborations are described below.

The duration of the individual projects of each Direct Participant differ. The activities have not started before the companies made their request for financial assistance to the national public authorities. The activities will start in XXX for the first of them. In any case, the effective implementation of State aid by national authorities remains subject to the prior approval of the Commission.

The activities of some of the Direct Participants will last until XXX.

**Table XX** below describes the expected timeline of the four WS. The end date of each WS is determined in relation to the end date of the works of the most distant individual project.

**Table XX: Timeline**

| **WS** | **Starting date** | **End date** |
| --- | --- | --- |
| WS SENSE | This WS will start in XXX as soon as the Commission issues its clearance decision. | Collaborations within this WS and/or with other WS are expected to terminate at the latest in XXX. |
| WS THINK | This WS will start in XXX as soon as the Commission issues its clearance decision. | Collaborations within this WS and/or with other WS are expected to terminate at the latest in XXX. |
| WS ACT | This WS will start in XXX as soon as the Commission issues its clearance decision. | Collaborations within this WS and/or with other WS are expected to terminate at the latest in XXXX. |
| WS COMMUNICATE | This WS will start in XXX as soon as the Commission issues its clearance decision. | Collaborations within this WS and/or with other WS are expected to terminate at the latest in XXX. |
| WS TRANSFORM |  |  |

It stems from the above that the different individual projects that constitute the components of the Integrated Project are inserted in a common roadmap aiming at the same objectives and are based on a coherent systemic approach in accordance with pt. 13 of the IPCEI Communication.

### 2.9.2 Necessity of the overall project and the sub-projects for Europe

… effort to reinforce the processor and semiconductor ecosystem and to expand industrial presence across the supply chain, in order to address key technological, security and societal challenges …

… aim to establish advanced European chip design capabilities and production facilities progressing towards leading-edge nodes for data processing and connectivity …

A new geopolitical, industrial, and technological reality is redefining the playing field. In what has long been a global business, major regions are reinforcing their local semiconductor ecosystems with a view to avoiding excessive dependencies on imports.

Europe is increasingly dependent on chips produced in other regions of the world - notably those used for electronic communications, data-processing and compute tasks, including processors.

… to design and eventually fabricate the next generation of trusted, low-power processors, for applications in high-speed connectivity, automated vehicles, aerospace and defence, health and agri food, artificial intelligence, datacentres, integrated photonics, supercomputing and quantum computing …

… research and investment plans for processor design, deployment and fabrication that considers the full semiconductor ecosystem …

As a conclusion, it stems from the above that the individual projects constituting the Integrated Project are necessary and complementary and that the criteria of integration set out at pt. 13 of the IPCEI Communication is met.

## 2.10 Governance

### 2.10.1 Types of Participation

Direct (with notification) and indirect participants (without notification)

### 2.10.2 Governance Bodies

**Supervisory Board (SB)**: A Supervisory Board will have the mission to supervise the monitoring and implementation of the Integrated Project as a whole and to ensure the annual reporting and monitoring obligations that will be required by the Commission under the rules of the IPCEI on the basis of any relevant information to be provided by the facilitation group (“FG”). The focus of the implementation is on both the technical advancement and spill-over activities to disseminate these advances, which the Direct Participants have committed themselves. The SB must inform the general assembly (the “GA”) of the progress of the Integrated Project once a year and in case of any modification of the Integrated Project.

The SB is composed of:

* The Public Authority Board (the “PAB”), with representatives of the MS participating in the Integrated Project, each MS having one vote,
* the chair and the deputy of the Integrated Project and the coordinators of the WS (together constituting the FG). The SB may invite additional company representatives or advisors assuming other missions linked to FG duties, without voting rights,
* three representatives of the Commission (DG RTD, DG CNECT, DG TRADE) as observers and advisers without voting rights

The members of the PAB and the Commission’s representatives will be appointed respectively by the MS and the Commission. The SB will ordinarily meet twice a year, possibly by teleconferencing or videoconferencing. In addition, the SB may meet in extraordinary session to discuss any event relating to the Integrated Project, in particular regarding the entry of new Direct Participant(s) or the exit of a Direct Participant. The entry of a new Direct Participant (potentially funded by a MS or financing authority other than MS) into the Integrated Project is possible under conditions that will be decided on the first SB meeting and be published. To this end, the applying Direct Participant(s) will submit to the SB, via its MS, a file demonstrating that its individual project is an addition to the Integrated Project’s work program, fits into its scope and schedule and proposes at least two collaborations with at least two existing Direct Participants. The same rules will apply to any additional individual project of an existing Direct Participant funded by a MS other than the current seven MS.

The MS of the applying Direct Participant will provide evidence that:

* it has carried out the necessary steps to ascertain from the Commission that the individual project meets the eligibility criteria for IPCEI laid out in the IPCEI Communication, in particular, but not limited to, the required innovation and RDI content, the contribution to spill-over and the evidence that the proposed works go beyond the state-of-the-art at the time of submission on the basis of public information;
* it is willing to bridge the funding gap or a reasonable fraction thereof, thus rendering the individual project viable, with suitable aid instruments in compliance with the IPCEI rules.

The entry of a new Direct Participant to the Integrated Project will be decided under conditions that will be fixed at the unanimity on the first SB meeting. The effective admission of the new Direct Participant is conditional upon the clearance of the related notification documents by the Commission, which needs to be submitted by the concerned MS (portfolio and adjusted Chapeau text) and all the other MS represented at the SB (adjusted Chapeau text).

A Direct Participant unexpectedly deciding to exit the Integrated Project (i.e. for other reasons than the end of its individual project as described in its portfolio) will inform the SB, via its respective concerned MS, of its withdrawal decision. The GA will take note of the exit decision either at the next ordinary GA meeting or by written consultation, teleconferencing or videoconferencing. With reference to the principle of protection of legitimate expectations and the principle of legal certainty, the exit of a Direct Participant will not impact the public support that each remaining individual project can benefit from at the date of the decision of the Commission clearing the contemplated Integrated Project. Should the exit of one or more Direct Participant reduce substantially and materially the objective and/or scope of one of the remaining active individual projects, the impact on the public support will be analysed at the level of the individual project concerned on a case by case basis.

To demonstrate the effectiveness of the Integrated Project setting and functioning, KPIs will be agreed upon at the first meeting of the SB and monitored accordingly in the course of the Integrated Project.

**IPCEI General Assembly (GA)**: Once a year, the IPCEI GA gathering all Direct Participants and the representatives of the IPCEI MS (and the Commission as observer) will be organized. The members of the IPCEI GA, other than the MS, will elect the members of the FG. In particular the GA elects the chair and the deputy of the Integrated Project and the coordinators of the WS, who will be members of SB. Each Direct Participant has one vote, decision of GA are taken with 2/3 majority.

At the first IPCEI GA (to be convened within four months after the decision of approval by the Commission), the chair and the deputy of the Integrated Project, the coordinators of the WS and their substitutes shall be designated officially. Detailed rules on the renewal and the duration of their term of office will be decided during this first IPCEI GA.

A Direct Participant member of the FG will be designated as key contact for the implementation of the spill-over commitments.

The GA is an internal meeting for the Direct Participants only, but from its second meeting onwards it shall be organized alongside the annual public IPCEI conference. At each GA conference, it will be decided on which MS organizes the next conference and the location where the next conference will be held. As mentioned below, the first conference will be organized by MS or … to take place on the XX-XX Month in Country.

**Facilitation group (FG)**: In a first approach, the FG shall be composed of:

* a chair and the deputy for the overall Integrated Project,
* the coordinators of the WS and their substitutes,
* and additional company representatives or advisors assuming other missions linked to the FG duties.

A specific focus on FG missions will be studied and proposed to highlight the effectiveness of its assigned tasks (i.e. WS coordination, annual reporting, communication, events preparation, etc.). Within the limits set by competition law, the FG will facilitate the sharing of information across Direct Participants which work on collaborations of similar nature and objective.

The FG drives the overall progress of the WS on a non-confidential basis to establish a permanent interface between private and public stakeholders with the goal to highlight the Integrated Project’s role and impact.

Up until the first SB, the following persons (lead/deputy) commit to work in the interim FG:

* [List of the companies’ representatives in the chapeau text design] + Others to be design

The members of the FG will evolve in time to take into consideration the end of participation of the Direct Participants according to their respective individual portfolio. Respective decisions on changes of the FG composition will be taken by the GA. The governance structure of the IPCEI on ME/CT is summarized in Figure XX below

The individual projects of the Direct Participants are governed by funding agreements with their relevant funding authority within each MS. Such funding agreements impose requirements and obligations regarding the administration of any individual project according to the rules set-up by the funding authority.

The national funding authorities are in possession of the commitments of all Direct Participants. As such, the PAB will be responsible for the monitoring of the completeness of the listings and announcements of the committed spill-over activities.

(Integration of the downstream industry, e.g. as a monitoring body; interface to the European Industry Alliance ….)

### 2.10.3 National Governance

## 2.11 Reporting

The FG is responsible for organizing and fostering the collaboration and the communication within the Integrated Project and vis-à-vis third parties which can benefit from results of the Integrated Project but are not Direct Participants. For this, two instruments will be implemented by the FG:

* the annual IPCEI meeting on ME/CT (2.11.1),
* the IPCEI website which will be set-up after the clearance decision (2.11.2).

### 2.11.1 Annual IPCEI ME/CT Meeting

The IPCEI meeting on ME/CT will take place once a year. The first meeting will take place at the latest one year after the date of the clearance decision of the Commission. During the first part of this meeting, a restricted session will be dedicated only to the MS, the Commission, and the Direct Participants. During this first session, each WS coordinator (the “WSC”) will present a slide deck on the overall activities of its WS. Each Direct Participant will present in more details the main results of its works and of the collaboration he participates to in the framework of the Integrated Project (subject to the protection of business secrets). Each Direct Participant will also describe in a slide deck the spill-over activities he participated to during the past year.

These slides decks will be based on a single template that will be defined by the SB during its first meeting. They will be gathered in a single document that will constitute the annual report on the activities of the Integrated Project. These slides decks do not replace the individual reports which have to be delivered by each Direct Participant to their respective national funding authorities.

The second part of the meeting will be a public conference open to any interested party and not limited to the Direct Participants during which they will present the main results of their works, subject to the protection of business secrets

### 2.11.2 IPCEI ME/CT website

The website will host public information about the Integrated Project and the Direct Participants. Moreover, the website will serve as the dissemination and interaction channel of the Integrated Project to engage with entities other than the Direct Participants. For this, the website will list all spill-over activities to which the Direct Participants have committed themselves. This information will be presented in form of an “Events Calendar” with the concrete dates and a brief description of the activity. The interested community will have the opportunity to register for participation at the activities directly with the Direct Participant who oversees the specific activity. The website will thus also serve as a basis for the annual reporting on the delivery of the committed activities. The FG will collect qualitative and quantitative information for each activity.

It may foresee a restricted area for Direct Participants only to organize the implementation of the Integrated Project.

# 3 Major Innovative Nature of Project

## 3.1 Major common results

The Integrated Project will bring forward innovation in all areas of the XXXX value chain. The section below summarizes, at the level of the Integrated Project, the innovations that are described at individual project-level in Section 2-1 above and, with more details, in each individual portfolio.

## 3.2 Major innovative nature of WS Sense

### 3.2.1 Innovative content of the WS Sense

### 3.2.2 Expected results of the WS Sense

The challenges of this WS will be addressed in the individual projects of the Direct Participants in different ways. The main outcome and expected results both in RDI and FID of WS Sense contributing to meet the overall objective are as follows.

Key expected results of WS Sense RDI activities are:

* ..

Key expected results of WS Sense FID activities are:

* …

## 3.3 Major innovative nature of WS Think

### 3.3.1 Innovative content of the WS Think

### 3.3.2 Expected results of the WS Think

The challenges of this WS will be addressed in the individual projects of the Direct Participants in different ways. The main outcome and expected results both in RDI and FID of WS Think contributing to meet the overall objective are as follows.

Key expected results of WS Think RDI activities are:

* ..

Key expected results of WS Think FID activities are:

* …

## 3.4 Major innovative nature of WS Act

Work package 2 within this workstream is of a major innovative nature due to the technical advantage of compound semiconductors compared to conventional Si semiconductors.

Semiconductors are materials that have a gap between the top of the valence band and the bottom of the conductor band (insulators have very large gap between the bands, conductors have overlapping bands). The larger this “bandgap” is, the higher is the performance of the semiconductor. Compound semiconductors such as SiC or GaN have a larger bandgap than Si semiconductors. The larger bandgap of compound semiconductors results in lower energy losses and reduced system size as a result of decreased cooling requirements and the need for passive components. For example, SiC modules can produce the same or better results using less space in an electric driveline compared to Si semiconductors. As automakers develop EVs operating at higher voltages in order to enable higher performance and extended ranges, SiC MOSFETs – in addition to being smaller and lighter than Si alternatives – offer a number of technological advantages.

Furthermore, the use of SiC technology in compound semiconductors has a particularly positive impact on the environment as it allows for a more efficient energy use compared to Si semiconductors. Due to a significant cost advantage and increase in performance, SiC will promote the transition from common combustion vehicles to EVs on the customer side. The high voltage battery in an EV represents the largest single cost item in an EV. The capacity of the EV’s battery will determine both its cost and the vehicle range it can support on a single charge. Efficiency in the power semiconductors has a direct impact on the capacity required for the EV. Power converted more efficiently means a smaller capacity battery is required to reach the same range, or the range of a battery of the same size will be increased. Both are highly desirable from an OEM’s perspective.

### 3.4.1 Innovative content of the WS Act

### 3.4.2 Expected results of the WS Act

The challenges of this WS will be addressed in the individual projects of the Direct Participants in different ways. The main outcome and expected results both in RDI and FID of WS Act contributing to meet the overall objective are as follows.

Key expected results of WS Act RDI activities are:

* ..

Key expected results of WS Act FID activities are:

* …

## 3.5 Major innovative nature of WS Communicate

### 3.5.1 Innovative content of the WS Communicate

### 3.5.2 Expected results of the WS Communicate

The challenges of this WS will be addressed in the individual projects of the Direct Participants in different ways. The main outcome and expected results both in RDI and FID of WS Communicate contributing to meet the overall objective are as follows.

Key expected results of WS Communicate RDI activities are:

* ..

Key expected results of WS Communicate FID activities are:

* …

## 3.6 Major innovative nature of WS Transform

### 3.6.1 Innovative content of the WS Transform

### 3.6.2 Expected results of the WS Transform

The challenges of this WS will be addressed in the individual projects of the Direct Participants in different ways. The main outcome and expected results both in RDI and FID of WS Transform contributing to meet the overall objective are as follows.

Key expected results of WS Transform RDI activities are:

* ..

Key expected results of WS Transform FID activities are:

* …

## 

# 4 The Importance of the IPCEI ME/CT

## 4.1 Size/Budget of the Project

The Integrated Project is large in scope given that it gathers XX companies within the EU and will cover the entire XXX value chain. It therefore meets the condition of quantitative importance of pt. 24 of the IPCEI Communication.

In addition, the IPCEI implies a considerable level of technological and financial risks, as evidenced by the confidential documents provided by each Direct Participant. It therefore also meets the condition of qualitative importance of pt. 24 of the IPCEI Communication.

The planned budget (see **Section 7**) clearly illustrates its large financial dimensions.

## 

## 4.2 Risk of the Project

The technologies in the framework of the Integrated Project are breakthrough and disruptive ones. The various phases from RDI to FID are very risky (technically, financially, and commercially) and encounter many barriers.

The Integrated Project faces many major risks, as of today’s assessment, that may have an impact on timing, profitability and even IPCEI’s features as currently designed. This is due to the magnitude, timing and ambition of the IPCEI.

The Integrated Project will also be confronted to **technological risks**: XXX

The Integrated Project will face **industrial risks** XXX.

The Integrated Project will face **financial risks** XXX

The Integrated Project will be confronted to **strategic and organizational risks**: XXXXX

The Integrated Project will also face **human resources risks**: XXXX

The Integrated Project will face **regulatory risks** XXXX

The Integrated Project will also face risks related to **major and innovative** programs: its duration and technological ambitions expose it to risks that are not all identifiable and/or quantifiable *ex ante*. It is conceivable that the initial schedule or the estimated budgets will not be respected, these two risks being associated insofar as each year of delay would generate significant additional costs.

## 4.3 Environmental Impact

Classification of the project and influence on the European carbon footprint and, if necessary, countermeasures (e.g. for investment measures).

For example, impact on:

a) **sourcing policies** shall be based on strict criteria reflecting the environmental protection principles already in place in the EU, as well as social protection principles thanks to EU legislation and EU shared societal values.

b) Cost effective and efficient **recyclability** targets for rare metals shall be an explicit project objective.

c) Storage products and systems shall be designed with a view to minimize their **CO2-eq footprint** throughout the whole life cycle of the product, from cradle to grave.

Environment protection during cell production will be ensured both by the existing legislation regulating large production sites and by the Integrated Project’s key intrinsic goals:

**existing regulation:**

**Integrated Project’s key intrinsic goals:**

**Integrated Project’s intrinsic goals regarding an increased sustainable use of raw materials and circular economy:**

# 5 Dissemination and positive spill-over effects

## 5.1 Overview of the dissemination and spill-over strategy of non-protected results

The Direct Participants to the Integrated Project will disseminate knowledge that is not protected by IP rights (“**IPR**”) to the scientific community and the industry.

Different dissemination levels, ranging from awareness to exploitation, are proposed to ensure the translation of developments and outputs into new findings and market opportunities. The objective is to reach a wide range of potential users and uses among research, social, investment and policy makers.

A mapping of the dissemination actions of the non-protected results of the Integrated Project within the EU is presented in **Table XX** below.

**Table XX:** Matrix of the dissemination and spill-over strategy of non IP-protected results

| **Targeted audience** | **Purpose** | **Dissemination material vehicles** |
| --- | --- | --- |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

**Table xx** below details in a quantitative manner, the dissemination actions envisaged within the Integrated Project by the Direct Participants.

**Table xx: KPIs for dissemination and spill-over knowledge**

| **KPIs** | **Expected dissemination during the Integrated Project (estimates)** | **Difference with “business as usual” (estimates)** |
| --- | --- | --- |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

## 5.2 Participation to events

The Direct Participants will participate to conferences and public presentations in the framework of established international events listed in **Table XX** below.

These events cover several MS including (but not limited to): [List of the MS] etc. They are open to participants from all MS. They will therefore ensure wide geographic coverage, beyond the participating MS.

These events relate to several different sectors: [list of the relevant sectors], etc. They go largely beyond the sector where each Direct Participant operates. They will therefore ensure wide sector coverage.

**Table xx: Events/conferences where at least one Direct Participant will participate**

| **Name of event/conference**  **Frequency and locations**  **Main topics addressed** | **Connected mainly to Direct Participant(s)** |
| --- | --- |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

## 5.3 Dissemination and spill-over through the European collaborative RDI ecosystem

### 5.3.1 Dissemination through the scientific community

The Direct Participants to the Integrated Project commit to disseminate the IP-unprotected results acquired in the framework of the Integrated Project to the scientific community.

In particular, the Direct Participants will collaborate with the scientific community with indirectly involved partners which are described in a more detailed fashion in the portfolio of each Direct Participant but are presented above for each WS (see **Section 2-2-1**).

Among, and in addition to, the indirectly involved partners, the Direct Participants expect the following RTOs, described in **Table XX** below, to benefit from the dissemination of the results of the Integrated Project (this is an indicative and non-limitative list).

The Direct Participants will in particular finance and/or contribute to the creation/development of university/school chairs related to new materials, cells and system design with a view to train future European scientists, experts, engineers, technicians and operators. Through, among others, participation to excellence networks like XXXXX.

**Table xx: RTOs benefitting from Spill-over effects**

| **Name of RTOs** | **Country** |
| --- | --- |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

### 5.3.2 Dissemination and spill-over through the participation of Direct Participants to clusters

Results of the Integrated Project will be disseminated through the clusters to which the Direct Participants are members. It includes, for instance:

1. Clusters
2. Alliances
3. Etc.

Other clusters may be described by each Direct Participant in its respective individual portfolio.

### 5.3.3 Dissemination and spill-over through the participation of Direct Participants to professional associations

Professional associations will also constitute a network for dissemination. They include notably:

A close communication and connection to trade associations, chambers of commerce and other intermediary bodies (such as public employment services) will also constitute a way of dissemination.

As mentioned above, IP-unprotected results will be disseminated to the scientific community and the industry. Such dissemination effects will benefit many institutions and will not be limited to the industry where each Direct Participant is active.

### 5.3.4 Other dissemination

Direct Participants will cooperate with firefighters in the EU to help them gain knowledge and methodology on safety issues relating to the GEN 3 and GEN 4 cells and modules.

## 5.4 Dissemination and spill-over by IP-protected results diffusion

The Direct Participants will use several ways for disseminating IP-protected results. Below are provided some examples of dissemination. Additional details are mentioned in each individual portfolio.

## 5.5 Spill-over effects in FID

Within the timeframe of the Integrated Project, FID activities will lead to significant spill-over effects in downstream markets, among Direct Participants but also beyond them. Downstream participants will benefit in many ways from the FID phase. The Integrated Project will enable them to develop new product applications and designs and to acquire specific skills as well as know-how, which again can be used in cooperation with third parties (inside or outside the Integrated Project).

The Integrated Project will provide access to next generation XXXX, as well as to new technologies issued from FID phase to partners, LEs, SMEs and RTOs. This will be very helpful for SMEs and RTOs that want to develop new knowledge and applications considering the entire lifecycle of this high-performance XXXX. These partners will benefit of an early access to the latest technologies available and will be able to shorten their development time.

The FID phase will also generate spill-over effects to other industrial partners such as equipment manufacturers present all over Europe. Indeed, to support the FID phase, some technological progress will be needed from these industries. Therefore, they will benefit from their own feedback regarding RDI improving their own equipment, materials, and processes. This spill-over will be reinforced since the scope of Integrated Project is very large.

More specifically, the Direct Participants will use several ways for disseminating results during the FID. Below are provided some examples of dissemination. Additional details are mentioned in each individual portfolio.

Thus, the benefits of the FID phase are clearly not limited to the Direct Participants themselves but will also spill-over to the indirectly involved partners and expand to many EU high-tech industries, businesses and RTOs. The IPCEI on XXXX will therefore create positive spill-over effects on multiple levels of the value chain within the FID.

It stems from the above that the benefits of the Integrated Project are not limited to the Direct Participants but benefit the EU economy and society at large. These benefits are clearly defined in a concrete and identifiable manner, in accordance with pt. 17 of the IPCEI Communication

# 6 Participation of Several Member States

## 6.1 Member States Participating in Project

The above Figure XX depicts the direct participants and their headquarters within their member state. A total number of XX MS have selected XX companies in the context of the IPCEI ME/CT following a competitive, transparent, and non-discriminatory procedure. Moreover – in accordance with pt. 20.a) of the IPCEI Communication – the IPCEI ME/CT has been designed in a way that makes it possible for all interested MS to participate. All participating member states were invited to join two initial networking workshops, organised by the German coordinator, on XX April 2021 etc. Additionally. This illustrated the transparent and non-discriminatory scope of the integrated project as well as the fact that different types of individual projects with very different amounts of public support have been selected by the existing MS. The Integrated Project involves more than one MS in accordance

Each individual project is co-financed by each Direct Participant as described in their respective portfolios, in accordance with pt. 18 of the IPCEI Communication.

## 6.2 Member States Strategic Perspective

### 6.2.1 MALTA Strategic goal

Malta recognises the strategic and economic importance of the Microelectronics sector both at national level and on a European scale. The goal is to enforce and consolidate the innovation and competitiveness of some key industrial assets operating in MALTA in the field of Microelectronics back-end manufacturing and power electronics.

Through its participation in the IPCEI ME-CT, Malta aims to enforce and consolidate the innovation and competitiveness of some of its key industrial assets involved in back-end manufacturing operations. These assets are strategic to ensure EU sovereignty and future autonomy on key microelectronics back-end capacity, that is in fierce competition vs. far east.

Support for the implementation of these strategic projects is essential to maintain our stakeholder’s advanced position in the sector. According to the Maltese government, this strategy is perfectly in line with the IPCEI ME-CT.

# 7 Necessity and proportionality of the aid

## 7.1 State Aid Measures

The notified measure is a case of application of the IPCEI Communication

## 7.2 Aid granting chronology

The activities that the national authorities intend to support have not started before the companies made their request for assistance to the public authorities. In any event, the effective implementation of State aid by the national authorities remains subject to the prior approval of the Commission.

MS will pay the aid according to the expenditures incurred within the ceiling of the aid provided for in Annexes below. If an advance payment is required to start the work of a Direct Participant, the MS may make an advance payment under the financing agreement to be concluded with him.

Once a year, during each individual project, the MS shall verify, for each Direct Participant, that the amount of aid granted does not exceed (or in the case of an advance, covers) the amount of eligible expenditure actually incurred for the purpose of advancing the individual project within the limits of the State aid ceilings

## 7.3 Claw-back mechanism

## 7.4 Aid granting procedure

### 7.4.1 Cost and state aid

The table in Annex XX gives an overview of the overall State aid by MS. The details of State aid granted by MS are provided separately by each MS. The Integrated Project involves considerable co-financing by the beneficiaries as described in the individual portfolio of each Direct Participant. It therefore also meets the condition of co-financing set at pt. 18 of the IPCEI Communication.

### 7.4.2 Funding gap calculation

For a detailed calculation of the funding gap and the planned aid amounts, please refer to the confidential documents submitted for each beneficiary.

**Counterfactual scenarios**: Due to its exceptional size and the synergies it requires from the various partners, this Integrated Project could not be achieved by industry alone, and such technological breakthroughs could not be created. Without the help of the MS involved in the financing of this Integrated Project, the Direct Participants would have focused on their own roadmaps to the detriment of innovations whose spill-over effects will largely benefit European ecosystems.

Detailed information is to be found in the individual portfolios on:

* the incentive effect and the proportionality of the public support,
* the limited effects on competition,
* the absence of overcapacity (aggregated information the expected capacity is provided above, pts. 15 et seq.).

**Necessity and proportionality of the aid**: Each MS has defined its State aid model and assessment of necessity and proportionality is detailed at the level of each individual portfolio.

**Transparency**: The involved MS will ensure that all the transparency and publication requirements stipulated in points 45 and 46 of the IPCEI Communication will be met.

# ANNEX 1

Examples of concrete technology projects:

* **Semiconductors: Development and Manufacturing**
  + Semiconductor-grade polysilicon with improved purity wafer substrates (silicon and compound semiconductors),
  + Development and pilot scale production of large Compound Semiconductor Substrates (8” GaAs, 6” InP, 4” GaN)
  + high purity materials, precursors, and gases,
  + equipment needed for processor and other semiconductor production (memory) in advanced technology nodes (including ≤10nm)
  + equipment needed for advanced opto-electronic technologies (≤ 5µm LEDs and Laser),
  + FID at scale for wafer processing and post-fab operations including test and bump,
  + heterogeneous integration and packaging of chips plus subsequent system level integration
  + novel, down-scaled processors and memories including emerging memories, “beyond von Neumann” approaches (neuromorphic circuits, in- or near-memory-computing…), design and architectures as System-in-Package (chiplet) or System-on-Chip (embedded)
  + IC design (processor, memory macros, periphery components)
  + Safeguard critical supply chain for advanced materials in power-, RF-, opto-electronics and photonics
* **Power Electronics** 
  + Enhancing the state-of-art semiconductors in an energy efficient, highly compact, and small form-factor, switching module
  + integration of Power semiconductors with digital control and communication
  + Next-generation trench compound semiconductor devices and technologies
  + Equipment needed to produce the layer sequence of compound semiconductor
* **Semiconductors back-end manufacturing: assembly, packaging, and test** 
  + Back-End new plant targeting low eco-footprint facility (Carbon Neutral), green process treatments and bioremediation, water waste recycling, innovative materials and processes.
  + FID at scale to realize a high-volume Industry 4.0 state-of-the-art manufacturing Pilot line to boost the Back-End’s competitiveness in Europe versus the Far East, greater China and USA.
  + Digital control modelling for facilities and operations, advances fab automation, robotics to assist material management and tools loading, integrated supply chain (sub 7nm large dice SiP capability**).**
  + Artificial Intelligence (AI) and Machine Learning leveraging on big-data and data analytics, to improve manufacturing efficiency.
  + large frames and advanced packaging TQFP and FC BGA for automotive application.
  + Advanced System-in-Package engineering, manufacturing and test in Europe allowing the production of requested payload and terminal key components.
* **Development and manufacturing of the newest generation of SiC semiconductors**
  + Research on the integration of SiC semiconductor devices into a new, highly innovative electric vehicle (“EV”) power core ecosystem focused first on the automotive industry
  + Improvement of performance of SiC semiconductors in other applications to create wider acceptance of SiC technology
  + Optimization of efficiency of SiC semiconductors and electrical, thermal, magnetic and mechanical optimization to achieve max. cost efficiency
* Necessary analogy semiconductor components to test and develop upcoming communication components and equipment
* **Software and systems** exploiting the benefits of above microelectronics hardware (design of AI devices, neuromorphic algorithms, learning processes for neural networks, high-level system models, interfaces, compilers/assemblers, systems software for configuration and use of microelectronics for safe and secure systems)
* **Virtualized network functions development**
* **Open RAN end-to-end system development**
* **Target applications are e.g.**
* **Telecommunications (5G/6G/Wi-Fi):** Infrastructure solutions for network and base stations and edge communication devices based on reliable ubiquitous and sovereign 5G/6G/next-gen Wi-Fi technologies.
* Non-Terrestrial Networks (NTN) in 5G/6G: Semiconductors used to build new 5G direct access payloads for LEO satellites and to manufacture terminals
* Innovative processes and production equipment enabling the production of important strategic materials like layer stacks and single crystal SiC, GaN and single crystal sapphire for key industries in Europe (Automotive, Renewable energy, Communications, µLEDs etc.) to mitigate almost total dependencies from resources outside Europe (US, Asia)
* **Industry Sector/Industry 4.0:** New sensor technologies for advanced robotic applications, retrofitting to machines and systems
* **Mobility:** Sensor and actor systems for autonomous platforms, System solutions for ADAS applications and electric vehicles, charging infrastructure, increase vehicle range and performance; New feedback sensor technology for advanced motor technology, new sensor technology for improved object recognition
* **Cybersecurity and functional safety:** Quantum computer-secure next-generation cybersecurity technology, safety, and security along the value chain, including mixed-criticality systems, security for safety
* **AI/ML and Edge Computing** including IP generation
* **High-performance computing**
* **IoT**
* **Installation of EU based TIER1 supply for materials and chemical precursors**
  + Sustainable sourcing and production
  + Package & delivery
  + Circular economy / recovery from End-of-Life products

# Annexe 2

Presentation of the Direct Participant

[Presentation of the undertaking in one paragraph].

Presentation of the individual project

Presentation of the individual project that shall be sharable to all the participant if not the description shall contain [*beginning of confidential section*] blabla [*End of confidential section*]

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1. <https://www.consilium.europa.eu/media/48976/250321-vtc-euco-statement-en.pdf> [↑](#footnote-ref-2)
2. <https://digital-strategy.ec.europa.eu/en/library/joint-declaration-processors-and-semiconductor-technologies> [↑](#footnote-ref-3)
3. https://ec.europa.eu/commission/presscorner/detail/en/IP\_21\_983 [↑](#footnote-ref-4)
4. <https://digital-strategy.ec.europa.eu/en/news/member-states-join-forces-european-initiative-processors-and-semiconductor-technologies> [↑](#footnote-ref-5)
5. Cf. table X: Microelectronics Ecosystem Matrix in ANNEX 1 [↑](#footnote-ref-6)
6. Cf. chapter 1.3 [↑](#footnote-ref-7)
7. <https://ec.europa.eu/commission/presscorner/detail/en/IP_21_983> [↑](#footnote-ref-8)
8. C.f. Page 14 [↑](#footnote-ref-9)
9. Memorandum of Understanding on the Implementation of OPEN RAN based Networks in Europe [↑](#footnote-ref-10)
10. Cf. Horizon Europe’s first strategic plan 2021-2024: <https://ec.europa.eu/commission/presscorner/detail/en/ip_21_1122> [↑](#footnote-ref-11)
11. <https://digital-strategy.ec.europa.eu/en/library/joint-declaration-processors-and-semiconductor-technologies> [↑](#footnote-ref-12)
12. <https://digital-strategy.ec.europa.eu/en/policies/quantum> [↑](#footnote-ref-13)
13. <https://digital-strategy.ec.europa.eu/en/news/eu-pact-skills-upskilling-and-reskilling-initiative-those-training-and-working-microelectronics> [↑](#footnote-ref-14)